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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,417	03/08/2001	Hidekazu Watanabe	80398P348	5418

8791 7590 02/15/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
AUVE, GLENN ALLEN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 02/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/802,417	WATANABE, HIDEKAZU	
	Examiner	Art Unit	
	Glenn A. Auve	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-13,15-23 and 25-30* is/are rejected.

7)☒ Claim(s) *4,14 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant should note that the examiner in charge of this application has changed. The current contact information is included at the end of this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3,5,7-13,15,17-23,25 and 27-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Olarig, U.S. Pat. No. 6,175,889 B1.

As per claim 1, Olarig shows an apparatus comprising: first and second bus interface circuits to interface to first and second buses, respectively, the first bus being accessible to a first processor (fig.4, host bus 103 can be first bus with interface 422, and any of the PCI-X buses can be second bus with its associated interface); a processor interface circuit to interface to a second processor, the second processor having accessibility to the first and second buses (a PCI-X device on another of the buses is interfaced to have access to the other buses, PCI-X devices can be controllers, processors, or other devices); and an arbitration logic circuit (432) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors (cols. 17-21 describe the operation of the system shown in figs. 4). Olarig shows all of the elements recited in claim 1.

As for claim 2, the argument for claim 1 applies. Olarig also shows that the second processor is coupled to the first and second buses (a device on the PCI-X bus can be coupled to any of the other buses). Olarig shows all of the elements recited in claim 2.

As for claim 3, the argument for claim 2 applies. Olarig also shows that the processor interface circuit comprises: a command decoder to decode an access command from the second processor requesting access to one of the first and second buses (inherent in that the bus interface must be able to decode the signals arriving from its attached device). Olarig shows all of the elements recited in claim 3.

As for claim 5, the argument for claim 1 applies. Olarig also shows that the arbitration logic circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted (cols. 17-21). Olarig shows all of the elements recited in claim 5.

As for claim 7, the argument for claim 1 applies. Olarig also shows that the first processor is one of a microprocessor, a micro-controller, and a digital signal processor (102). Olarig shows all of the elements recited in claim 7.

As for claim 8, the argument for claim 1 applies. Olarig also shows that the second processor is a direct memory access (DMA) controller (the PCI-X device can be any sort of device including a DMA controller). Olarig shows all of the elements recited in claim 8.

As for claim 9, the argument for claim 1 applies. Olarig also shows that the first and second buses are of same type (The system could be interpreted such that instead of calling the host bus coupled to the CPU the first bus, any of the PCI-X buses could be considered the first bus coupled to a PCI-X device which could be a first processor. In that case the two buses would both be of the PCI-X type). Olarig shows all of the elements recited in claim 9.

As for claim 10, the argument for claim 1 applies. Olarig also shows that the first and second buses are of different types (as noted above for claim 1, first bus is the host bus and the second bus is PCI-X). Olarig shows all of the elements recited in claim 10.

As per claim 11, Olarig shows a method comprising: interfacing to first and second buses by first and second interface circuits, respectively, the first bus being accessible to a first processor; interfacing to a second processor, the second processor having accessibility to the first and second buses; and arbitrating access requests from the first and second processors (all as noted above for claim 1). Olarig shows all of the steps recited in claim 11.

As for claim 12, the argument for claim 11 applies. Olarig also shows that the second processor is coupled to the first and second buses (as above for claim 2). Olarig shows all of the steps recited in claim 12.

As for claim 13, the argument for claim 12 applies. Olarig also shows that interfacing to the second processor comprises: decoding an access command from the second processor requesting access to one of the first and second buses (inherent in that the bus interface must be able to decode the signals arriving from its attached device). Olarig shows all of the elements recited in claim 13.

As for claim 15, the argument for claim 11 applies. Olarig also shows that arbitrating access requests comprises enabling the first and second bus interface circuits when access request to the second bus from the first processor is granted (as above for claim 5). Olarig shows all of the steps recited in claim 15.

As for claim 17, the argument for claim 11 applies. Olarig also shows that the first processor is one of a microprocessor, a micro-controller, and a digital signal processor (as above for claim 7). Olarig shows all of the steps recited in claim 17.

As for claim 18, the argument for claim 11 applies. Olarig also shows that the second processor is a direct memory access (DMA) controller (as above for claim 8). Olarig shows all of the steps recited in claim 18.

As for claim 19, the argument for claim 11 applies. Olarig also shows that the first and second buses are of same type (as above for claim 9). Olarig shows all of the steps recited in claim 19.

As for claim 20, the argument for claim 11 applies. Olarig also shows that the first and second buses are of different types (as above for claim 10). Olarig shows all of the steps recited in claim 20.

As per claim 21, Olarig shows a system comprising: first and second buses (103,206); first and second processors (CPU 102 and a processor or controller coupled to the PCI-X bus), the first processor being coupled to the first bus (102/103); a bus controller coupled to the first and second buses to control bus access from the first and second processors (204), the bus controller comprising: first and second bus interface circuits to interface to the first and second buses (fig.4), respectively, a processor interface circuit to interface to the second processor (a PCI-X device on another of the buses is interfaced to have access to the other buses, PCI-X devices can be controllers, processors, or other devices), the second processor having accessibility to the first and second buses, and an arbitration logic circuit (432) coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors (see also cols. 17-21). Olarig shows all of the elements recited in claim 21.

As for claim 22, the argument for claim 21 applies. Olarig also shows that the second processor is coupled to the first and second buses (as above for claim 2). Olarig shows all of the elements recited in claim 22.

As for claim 23, the argument for claim 22 applies. Olarig also shows that the processor interface circuit comprises: a command decoder to decode an access command from the second processor requesting access to one of the first and second buses (inherent in that the bus interface must be able to decode the signals arriving from its attached device). Olarig shows all of the elements recited in claim 23.

As for claim 25, the argument for claim 21 applies. Olarig also shows that the arbitration logic circuit enables the first and second bus interface circuits when access request to the second bus from the first processor is granted (as above for claim 5). Olarig shows all of the elements recited in claim 25.

As for claim 27, the argument for claim 21 applies. Olarig also shows that the first processor is one of a microprocessor, a micro-controller, and a digital signal processor (as above for claim 7). Olarig shows all of the elements recited in claim 27.

As for claim 28, the argument for claim 21 applies. Olarig also shows that the second processor is a direct memory access (DMA) controller (as above for claim 8). Olarig shows all of the elements recited in claim 28.

As for claim 29, the argument for claim 21 applies. Olarig also shows that the first and second buses are of same type (as above for claim 9). Olarig shows all of the elements recited in claim 29.

As for claim 30, the argument for claim 21 applies. Olarig also shows that the first and second buses are of different types (as above for claim 10). Olarig shows all of the elements recited in claim 30.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1,6,11,16,21, and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Okazawa et al., U.S. Pat. No. 5,668,956.

As per claim 1, Okazawa shows an apparatus comprising: first and second bus interface circuits to interface to first and second buses (fig.7, connection controller 705 interfaces to buses 711 and 113), respectively, the first bus being accessible to a first processor (701); a processor interface circuit to interface to a second processor, the second processor having accessibility to the first and second buses (processor 703 is interfaced with the connection controller and can communicate with any of the other buses (col.5, line 65 - col.6, line 34); and an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors (the connection controller arbitrates or decides which buses are coupled to which other buses). Okazawa shows all of the elements recited in claim 1.

As for claim 6, the argument for claim 1 applies. Okazawa also shows that the arbitration logic circuit resolves access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus (the first processor can be coupled with the memory for example while the second processor is coupled with bus 113). Okazawa shows all of the elements recited in claim 6.

As per claim 11, Okazawa shows a method comprising: interfacing to first and second buses by first and second interface circuits, respectively, the first bus being accessible to a first processor; interfacing to a second processor, the second processor having accessibility to the first and second buses; and arbitrating access requests from the first and second processors (as above for claim 1). Okazawa shows all of the steps recited in claim 11.

As for claim 16, the argument for claim 11 applies. Okazawa also shows that arbitrating access requests comprises resolving the access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus (as above for claim 6). Okazawa shows all of the steps recited in claim 16.

As per claim 21, Okazawa shows a system comprising: first and second buses (fig.7, 711 and 113); first and second processors (701 and 703), the first processor being coupled to the first bus; a bus controller (705) coupled to the first and second buses to control bus access from the first and second processors, the bus controller comprising: first and second bus interface circuits to interface to the first and second buses, respectively, a processor interface circuit to interface to the second processor, the second processor having accessibility to the first and second buses, and an arbitration logic circuit coupled to the first and second bus interface circuits and the processor interface circuit to arbitrate access requests from the first and second processors (as above for claim 1). Okazawa shows all of the elements recited in claim 21.
As for claim 26, the argument for claim 21 applies. Okazawa also shows that the arbitration logic circuit resolves access requests from the first and second processors such that the first processor accesses the first bus while the second processor accesses the second bus (as above for claim 6). Okazawa shows all of the elements recited in claim 26.

Response to Arguments

6. Applicant's arguments, see pages 7-9 of the remarks, filed December 2004, with respect to the rejection(s)of claim(s) 1-30 under 35 USC §103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Olarig and Okazawa as applied above.

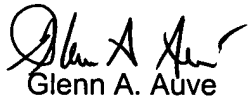
Conclusion

7. Claims 4,14, and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenn A. Auve whose telephone number is (571) 272-3623. The examiner can normally be reached on M-F 8:00 AM-5:30 PM, every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (571) 272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Glenn A. Auve
Primary Examiner
Art Unit 2111

gaa
14 February 2005